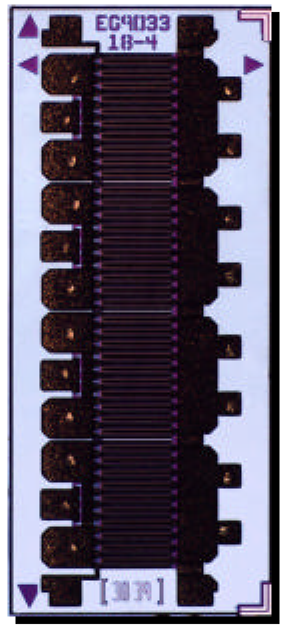
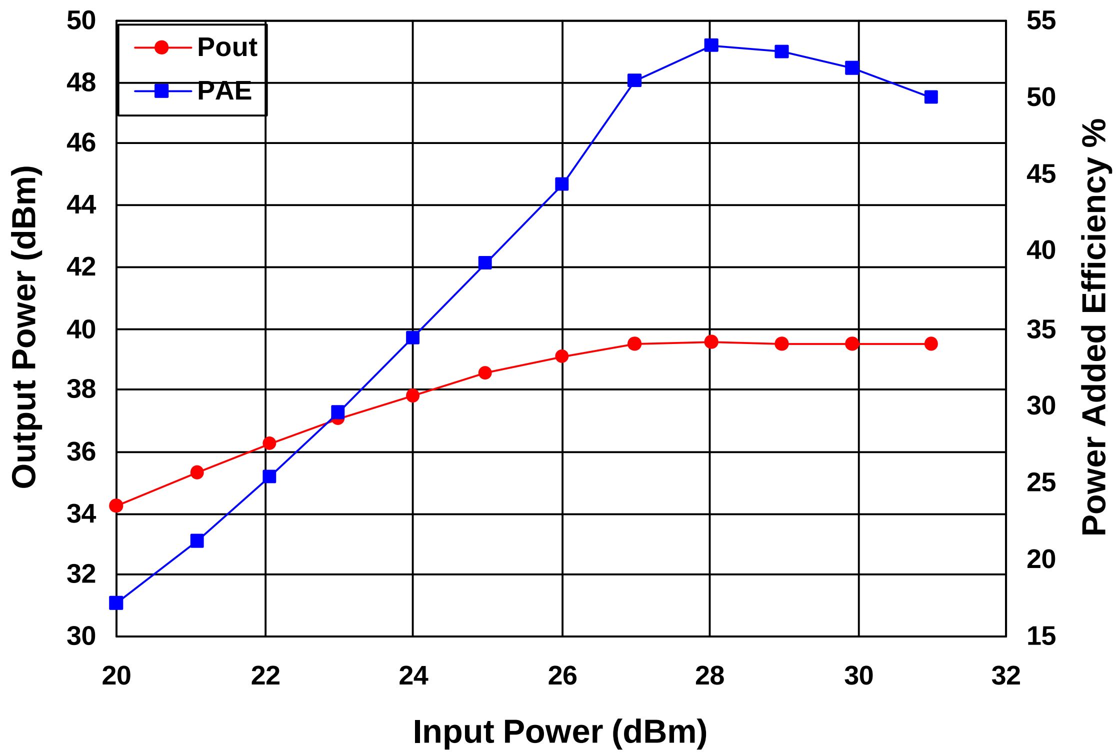
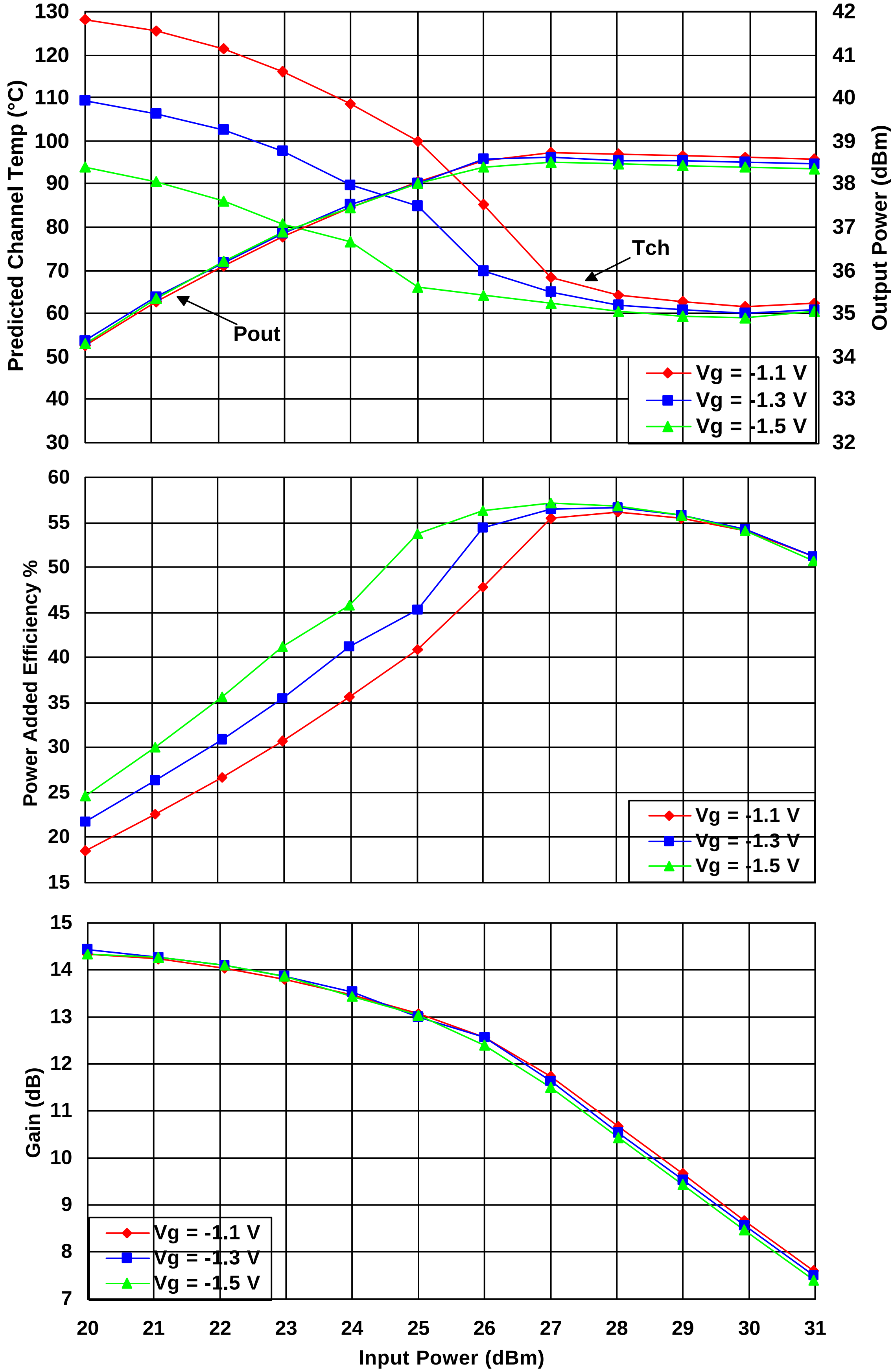


- **0.5 um gate finger length**
- **Nominal Pout of 9.0 Watts at 2.3 GHz**
- **Nominal PAE of 53% at 2.3 GHz**
- **Nominal Gain of 11.5 dB at 2.3 GHz**
- **Die Size 36.0 x 81.0 x 4.0 mils (0.914 x 2.057 x 0.102 mm)**

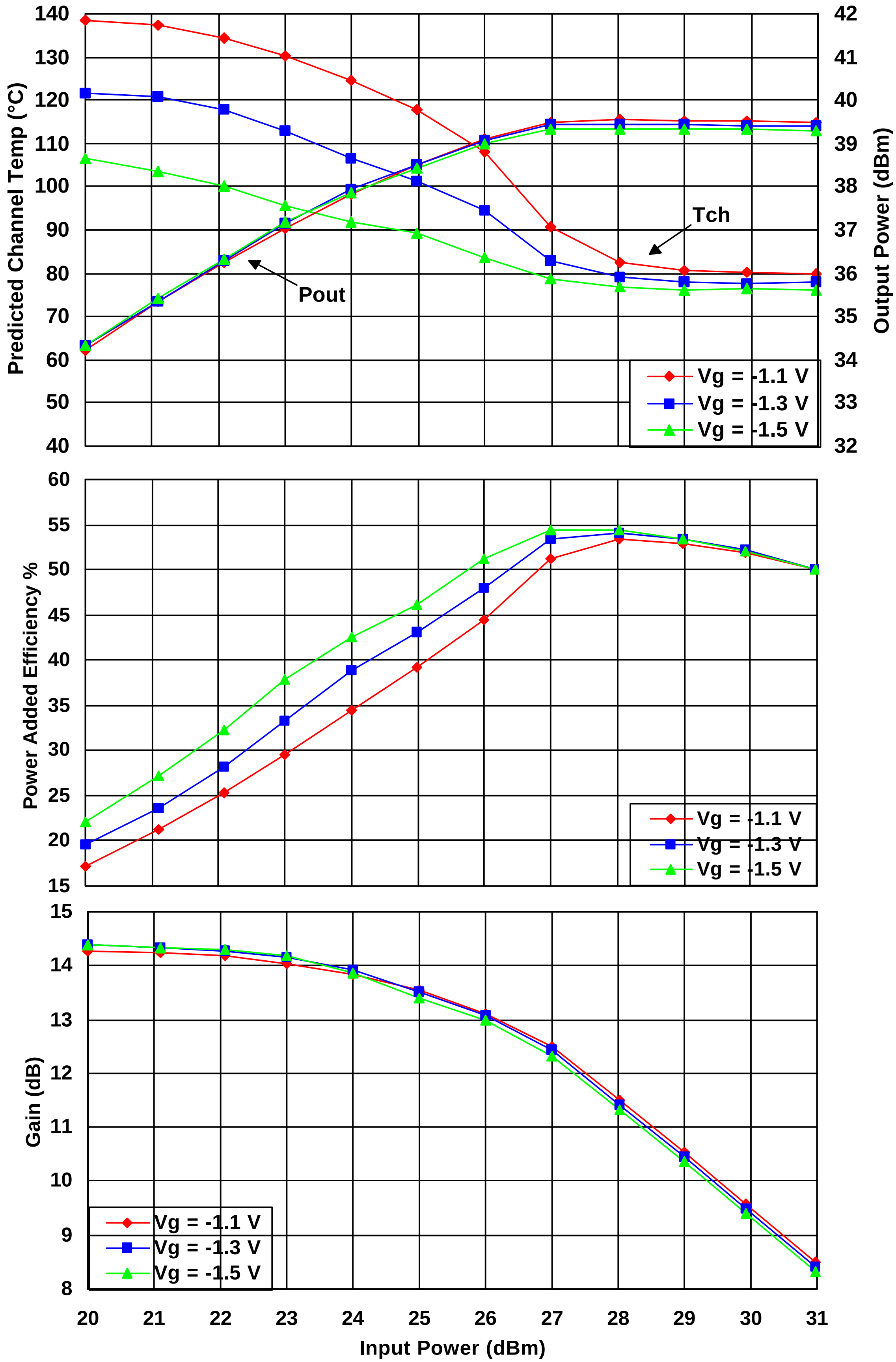
TGF4118-EPU RF Performance at F = 2.3 GHz
Vd = 8.0 V, Vg = -1.1 V, Iq = 1.69 A and T_A = 25°C



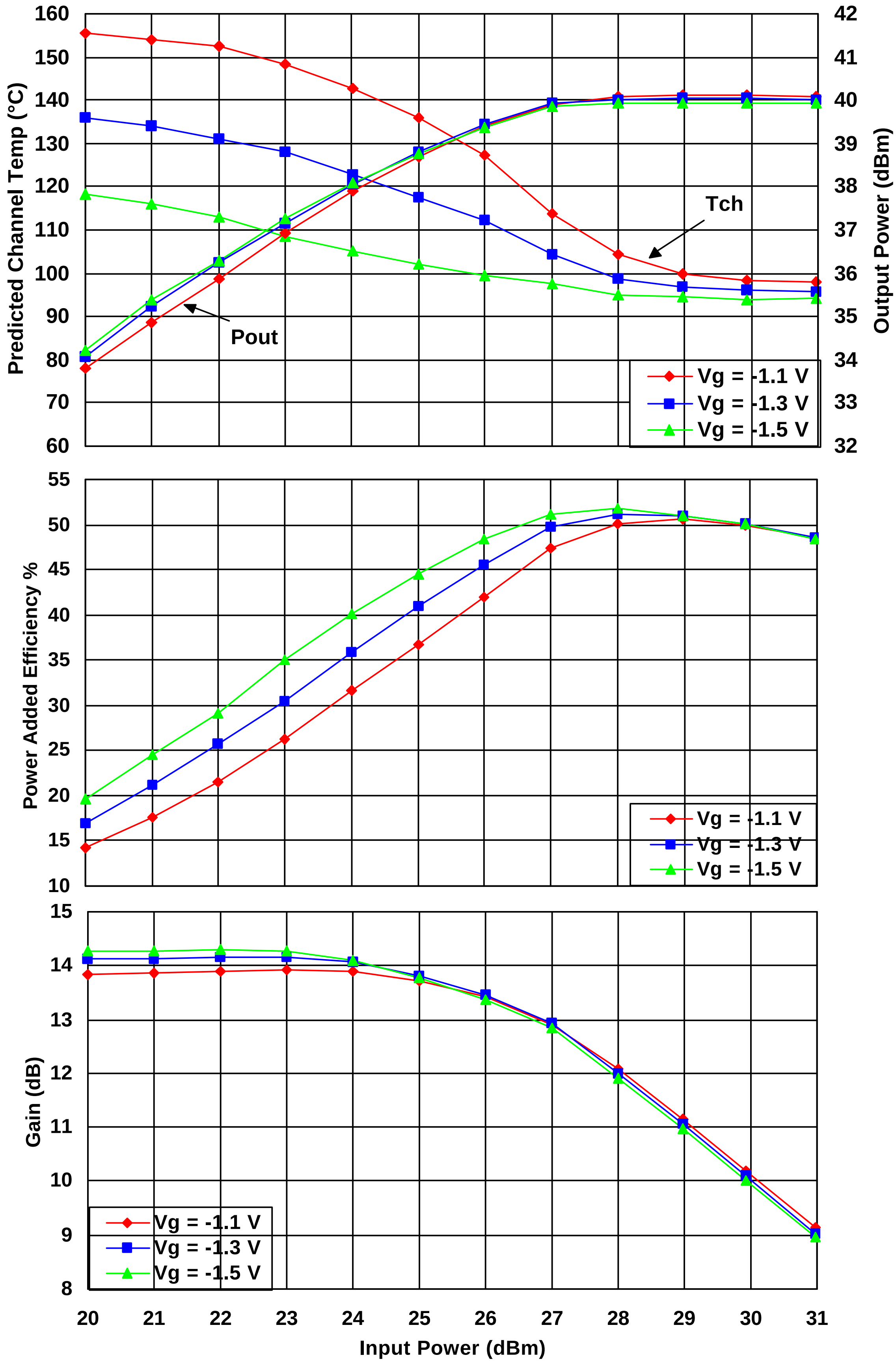
TGF4118-EPU RF Performance for Vd = 7.0 V, F = 2.3 GHz, and T_A = 25°C
Quiescent Id is 1.74 A (Vg = -1.1 V), 1.37 A (Vg = -1.3 V), and 1.02 A (Vg = -1.5 V)



TGF4118-EPU RF Performance for Vd = 8.0 V, F = 2.3 GHz, and T_A = 25°C
Quiescent Id is 1.69 A (Vg = -1.1 V), 1.38 A (Vg = -1.3 V), and 1.06 A (Vg = -1.5 V)



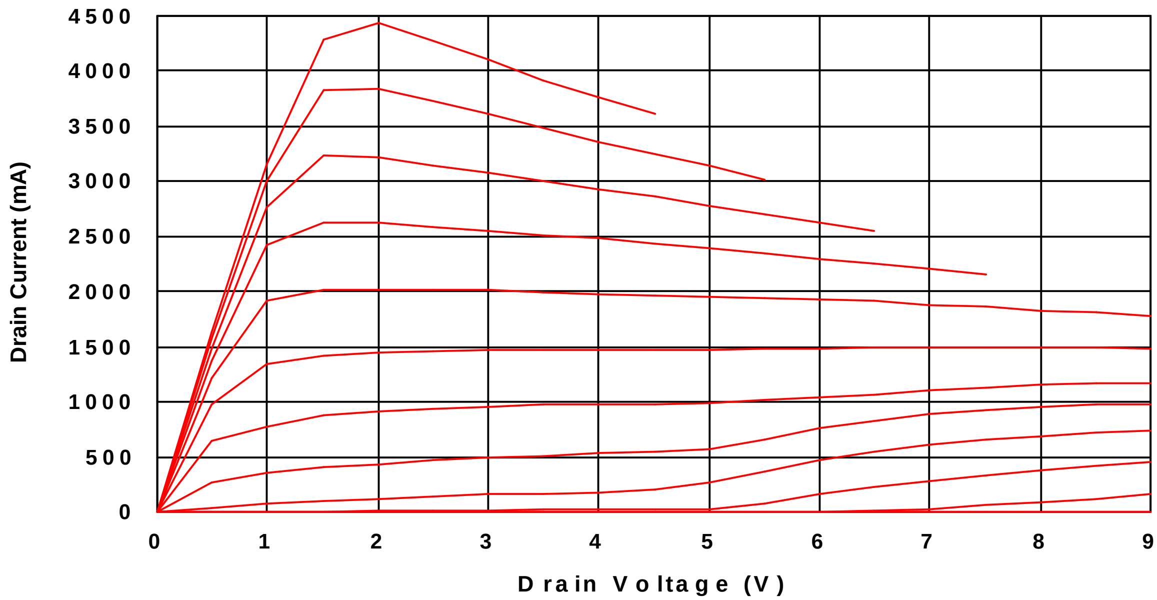
TGF4118-EPU RF Performance for Vd = 9.0 V, F = 2.3 GHz, and T_A = 25°C
Quiescent Id is 1.66 A (Vg = -1.1 V), 1.39 A (Vg = -1.3 V), and 1.09 A (Vg = -1.5 V)



DC Characteristics for the TGF4118-EPU

	DC probe Parameters	Nominal	Unit
IDSS	Drain Saturation Current	4410	mA
GM	Transconductance	2970	mS
VP	Pinch Off Voltage	-1.85	V
BVGS	Breakdown Voltage Gate-Source	-22	V
BVGD	Breakdown Voltage Gate-Drain	-22	V

Example of DC I-V Curves
Vg = 0.0 V to -2.75 V in 0.25 steps T_A = 25°C



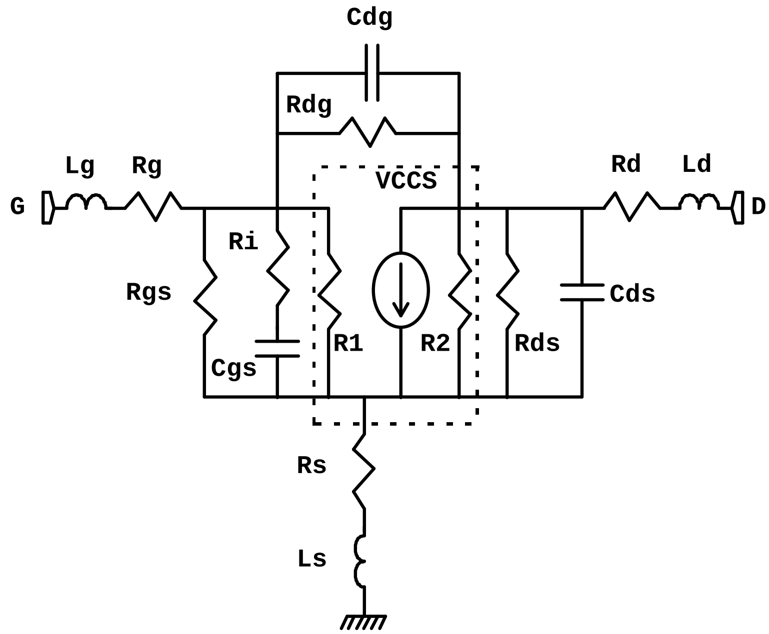
Absolute Maximum Ratings

Drain-to-source Voltage, Vds..12 V
Gate-to-source Voltage, Vgs..-5 V to 0 V
Mounting Temperature..320°C
Storage Temperature.. -65°C to 200°C
Power Dissipation..refer to Thermal Model
Operating Channel Temperature..refer to Thermal Model

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in this document is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

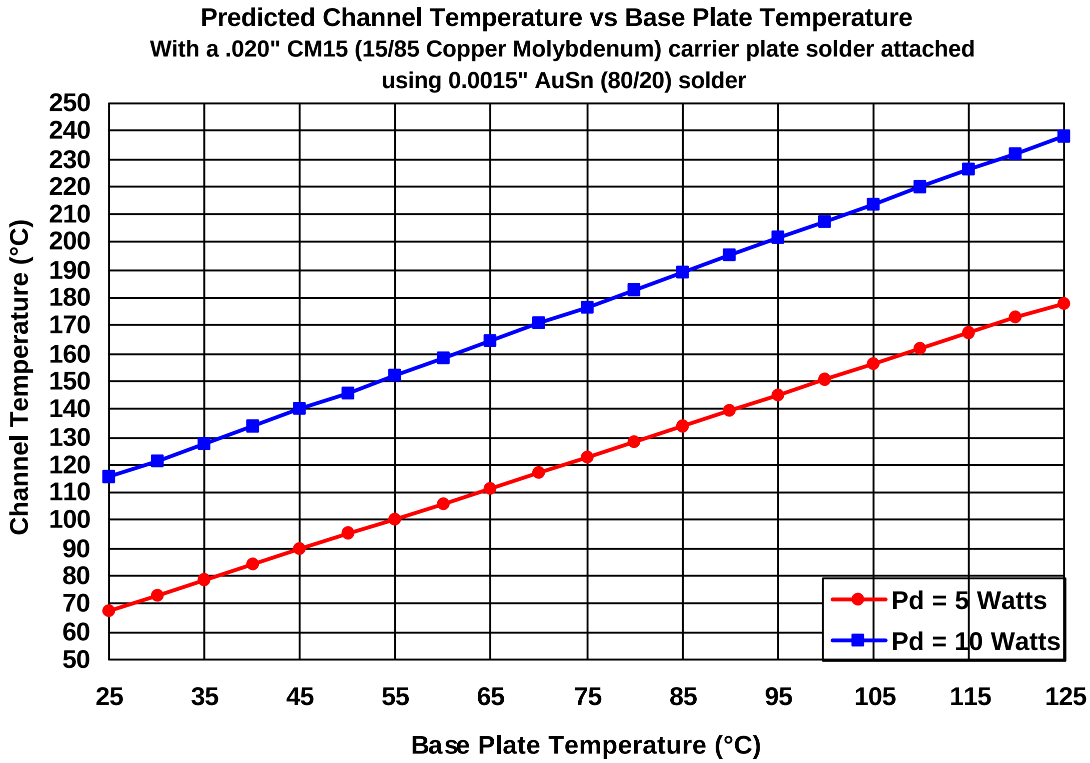
TGF4118-EPU Linear Model
Vds = 7 V and Ids = 1.24 A at T = 25°C

<u>FET Elements</u>
Lg = .00176 nH
Rg = 0.42115 Ω
Rgs = 5447 Ω
Ri = .05082 Ω
Cgs = 18.82602 pF
Cdg = 1.03674 pF
Rdg = 13600 Ω
Rs = 0.06265 Ω
Ls = 0.00869 nH
Rds = 6.40925 Ω
Cds = 3.72019 pF
Rd = 0.01831 Ω
Ld = 0.00195 nH
<u>VCCS Parameters</u>
M = 2.04398 S
A = 0
R1 = 1E19
R2 = 1E19
F = 0
T = 4.5116 pS

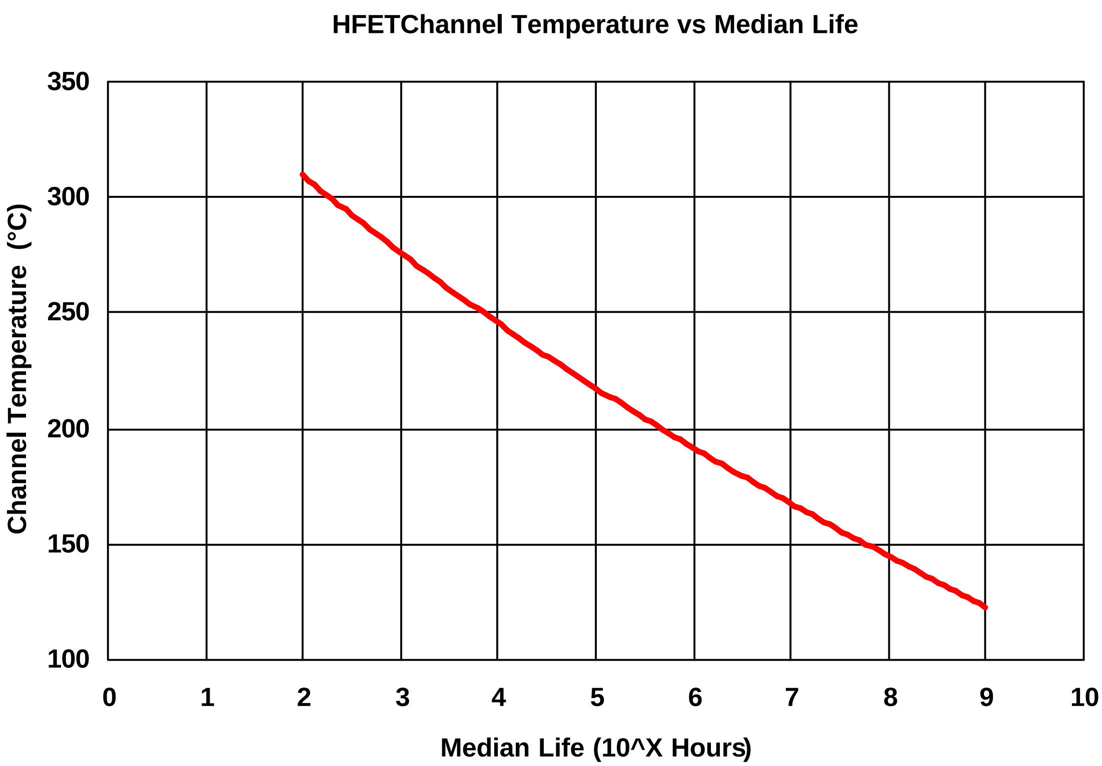


Freq-GHz	MAG-S11	ANG-S11	MAG-S21	ANG-S21	MAG-S12	ANG-S12	MAG-S22	ANG-S22
0.5	0.96061	-157.13	4.44294	98.2855	0.00932	14.7392	0.85196	-178.271
1	0.96275	-168.492	2.25188	88.8751	0.00949	13.5187	0.85594	-178.561
1.5	0.96332	-172.363	1.49968	83.3713	0.00955	15.8589	0.85818	-178.438
2	0.9637	-174.323	1.11963	78.9074	0.00962	19.1829	0.86065	-178.22
2.5	0.96407	-175.515	0.88979	74.9064	0.00971	22.9596	0.86355	-177.98
3	0.96446	-176.325	0.73541	71.1835	0.00985	26.9945	0.86689	-177.746
3.5	0.96488	-176.917	0.62432	67.6655	0.01003	31.1758	0.8706	-177.53
4	0.96532	-177.374	0.54038	64.3208	0.01028	35.4143	0.87462	-177.338
4.5	0.96579	-177.743	0.47464	61.1349	0.01058	39.6273	0.87887	-177.174
5	0.96628	-178.05	0.42171	58.1017	0.01096	43.7382	0.88328	-177.04

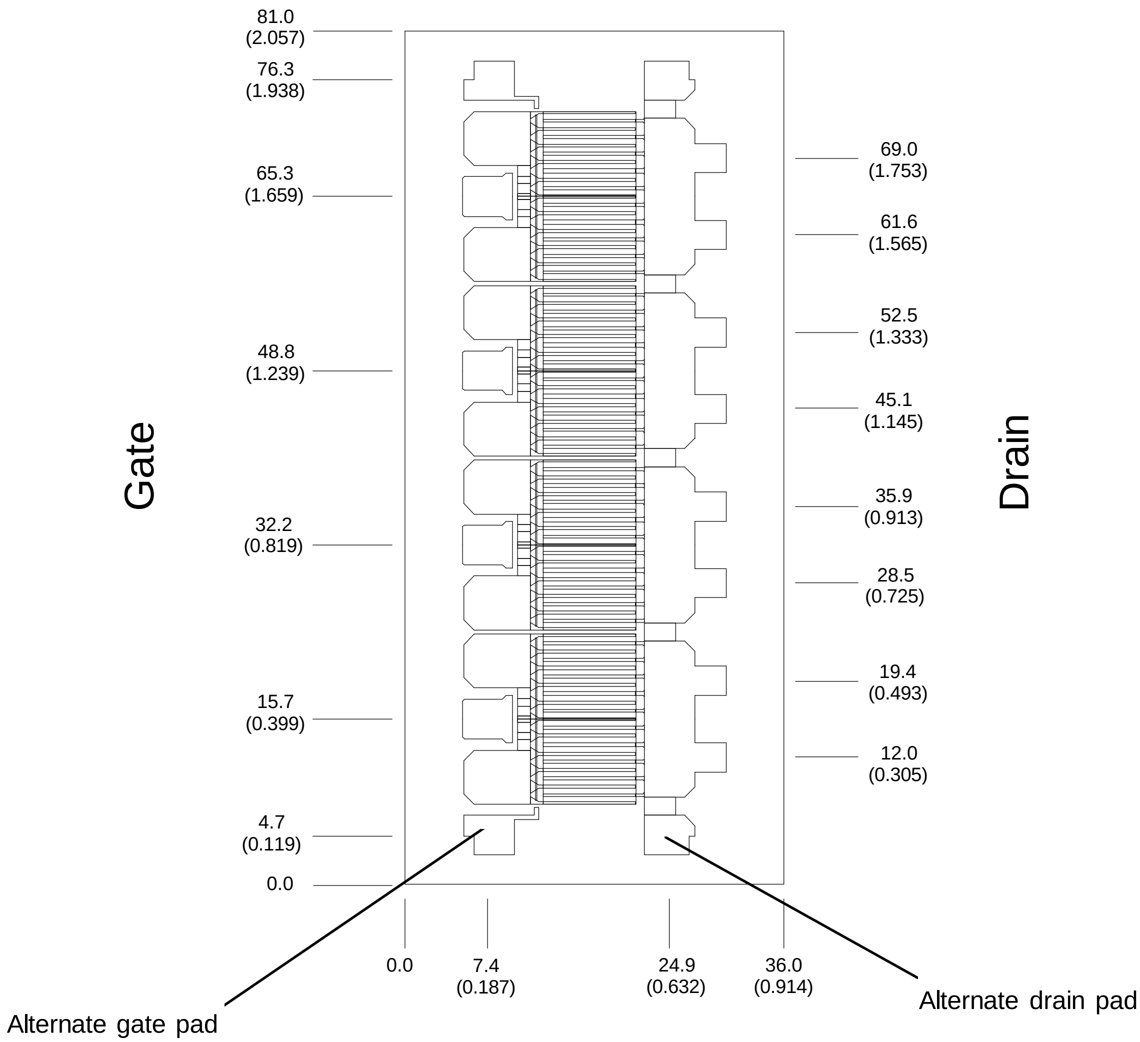
Thermal Model of TGF4118-EPU



Tc = 2.052 + 6.796 x Pd + 0.1465 x Pd ^{2} + (1.002 + 0.01999 x Pd + 0.0002725 x Pd ^{2}) x Tbase
(Predicted Channel Temperature equation for the given assembly stack up)
This model assumes perfect solder connections (no voids) between the FET and the carrier plate.

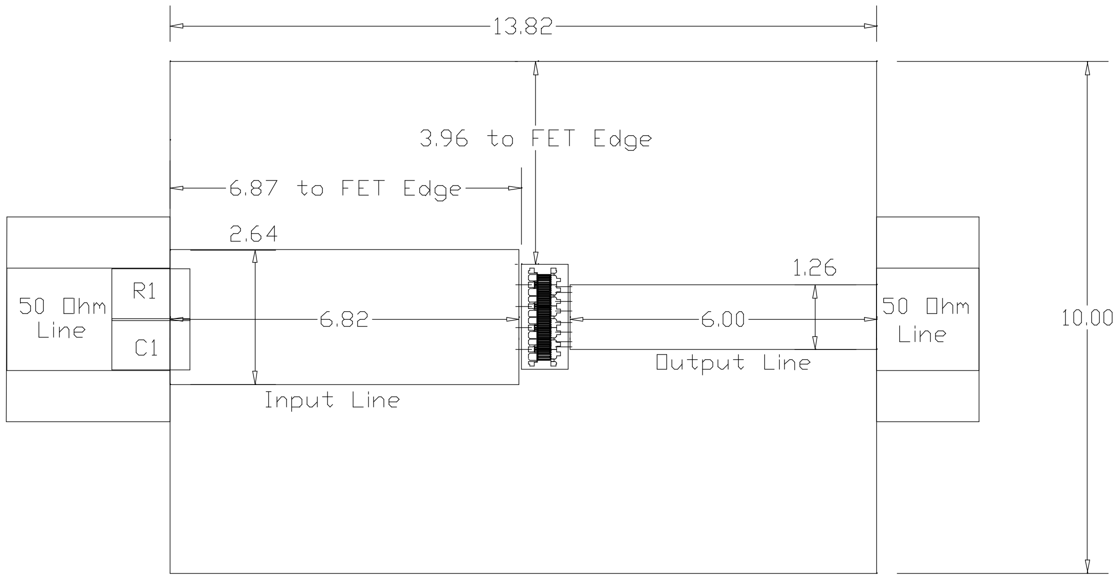


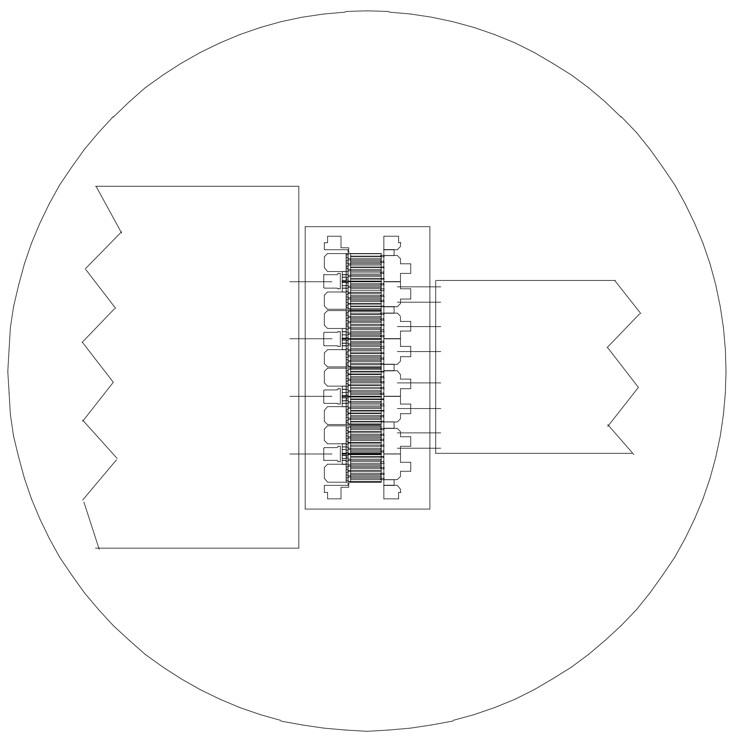
Mechanical Drawing of TGF4118-EPU



Units: mils (mm)
Thickness: 4.0 (0.10)
Gate pad sizes are 4.0 x 4.0 (0.10 x 0.10)
Drain pad sizes are 4.7 x 14.5 (0.12 x 0.37)
A minimum of four gate bonds and eight drain bonds is recommended for operation. Sources are connected to backside metalization. Alternate gate and drain pads are located on either end of the FET for paralleling TGF4118-EPUs.

Application circuit for the TGF4118-EPU at 2.3 GHz





The FET is soldered using AuSn solder at 300 C for 30 secs. Input and Output matching networks are 0.381 mm ZrSn Tioxide substrates (Er = 38). The design load impedance is between 4 Ω and 5 Ω with the 6 pF output capacitance of the FETincluded in the output network. For further explanation refer to the application note “Designing High Efficiency Amplifiers using HFETs”. The carrier plate is 0.51 mm gold plated copper molybdenum. Gold wire (0.018 mm) is used for the bonds. Four gate bonds are required with a length of 0.42 mm. Eight drain bonds are required with a length of 0.42 mm. Bondwire end points on the FET are in the middle of the bond pads. Refer to the figures above for bondwire locations. Connection between the 50 ohm line input to the input match is made by a parallel RC network. R1 in this network is 10 ohms, and C1 is 5.6 pF. The components used are surface mount 0603 piece parts.